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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,440	09/30/2003	Robert M. Geffken	BUR920030025US1	2439

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,440	GEFFKEN ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *17-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0903 & 1003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 09/30/2003 through 04/18/2005, claims 1-20 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 09/30/2003 an d10/27/2003. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

Election/Restriction

3. Application's election with traverse to prosecute the invention of Group I, claims 1-16, drawn to semiconductor devices, filed 04/18/2005 is acknowledged.

The traversal is on the ground(s) that see the election paper. This is not found persuasive because, first, the inventions are distinct, each from the other for the reason(s) set for in the restriction requirement. Second, the fields of search for method claims, which is classified in class 438, and device claims, which is classified in class 257, are NOT coextensive and the determinations of patentability of method and device

claims are different, that is process limitations and device limitations are given weight differently in determining the patentablitity of the claimed inventions. Also, the strategies for doing text searching of the device claims and method claims are different. Thus, separate searches are required.

The requirement is still deemed proper and is therefore made **FINAL**.

Claims 17-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected group there being no allowable generic or linking claim.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

4. Applicant is advised that a complete reply to this Office Action should include cancellation of nonelected claims or other appropriate action (37 CFR 1.144). See MPEP § 821.01. Also, upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).

Specification

5. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim(s) 1, 4 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent Application No. 2004/0097065 to Lur et al.

Regarding claim 1, Lur discloses a semiconductor device, as shown in figs. 13-11-12, comprising:

a first interconnect 28 adjacent a second interconnect 28 on an interconnect level;

spacers 14 formed along adjacent sides of the first and second interconnects 26 (paragraph [0067] and

an air gap 34 formed between the first and second interconnects 28, the air gap 34 extending above an upper surface of the interconnect 28 and below a lower surface of the interconnect 28, distance between the spacers defining the width of the air gap 28. See further paragraphs [0064]-[0067].

Lur also discloses all limitations of claim 4. See figs. 11-12 and paragraphs [0057], [0066].

8. Claim(s) 1-3 and 7-16 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,838,354 to Goldberg et al.

Regarding claim 1, Goldberg discloses a semiconductor device, as shown in figs. 7-8, comprising:

a first interconnect 44/30/18 or 98/90/88 adjacent a second interconnect 48a or 100 on an interconnect level;

spacers 67 (fig. 6) formed along adjacent sides of the first and second interconnects; and

an air gap 74/106 formed between the first and second interconnects, the air gap extending above an upper surface of the interconnect 44 or 98 and below a lower surface of the second interconnect 44 or 98, distance between the spacers 67 defining the width of the air gap 74/106.

Regarding claim 2, Goldberg discloses the semiconductor device wherein the air gap 74/106 is self-aligned to the adjacent sides of the first and second interconnects. See col. 15, lines 7-24.

Regarding claim 3, Goldberg discloses the semiconductor device wherein the spacers 67 adjacent the sides of the first and second interconnects comprise silicon dioxide or silicon nitride. See col. 3, lines 31-45.

Regarding claim 7, Goldberg discloses the semiconductor device further including hardmask spacers self-aligned to either side of an upper portion of the air gap. See fig. 5 and col. 4, lines 15-63.

Regarding claim 8, Goldberg discloses the semiconductor device wherein the hardmask spacers comprise silicon dioxide or silicon nitride. See fig. 5 and col. 4, lines 15-63.

Regarding claim 9., Goldberg discloses the semiconductor device further including at least one insulative layer 72 above the interconnect level and the air gap, and wherein the air gap extends into the insulative layer 72. See figs. 7-8.

Regarding claim 10, Goldberg discloses the semiconductor device wherein the at least one insulative layer above the interconnect level and the air gap comprises silicon

nitride or silicon carbon nitride as a capping layer for the interconnect and silicon dioxide or fluorinated silicon dioxide as an insulative layer above the capping layer. See col. 10, lines 9-44; col. 15, lines 8-28.

Regarding claim 11, Goldberg discloses the semiconductor device further including hardmask spacers self-aligned to either side of an upper portion of the air gap, and an insulative layer above the interconnect level, the air gap and the hardmask spacers, and wherein the air gap extends between the hardmask spacers and upward into the insulative layer. See figs. 7-8; and col. 10, lines 9-44; col. 15, lines 8-28.

Regarding claim 12, Goldberg discloses the semiconductor device wherein the first and second interconnects are formed by a damascene or dual damascene process. See col. 3, line 66 to col. 4, line 19.

Regarding claim 13, Goldberg discloses the semiconductor device wherein the first and second interconnects comprise copper, aluminum, tungsten or gold. See col. 3, lines 43-65.

Regarding claim 14, Goldberg discloses the semiconductor device further including, beneath one of the first and second interconnects, an etch stop layer positioned over at least one underlying via insulator level, and below the underlying via

insulator, a second interconnect level. See col. 6, lines 25-46; col. 9, lines 47-54; and col. 15, lines 8-28.

Regarding claim 15, Goldberg discloses the semiconductor device further including, between the at least one underlying via insulator level and the second interconnect level, a selective metal deposition layer comprising a selective tungsten layer or a selective cobalt tungsten phosphide layer. See col. 3, line 66 to col. 4, line 34.

Regarding claim 16, Goldberg discloses the semiconductor device further including, over each of the first and second interconnects, a selective metal deposition layer comprising a selective tungsten layer or a selective cobalt tungsten phosphide layer. See col. 3, line 66 to col. 4, line 34.

Claim Rejections - 35 U.S.C. § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim(s) 4-6 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,838,354 to Goldberg et al., in view of the following remarks.

Regarding claim 4, Goldberg discloses the semiconductor device further including, beneath the at least one of the first and second interconnects, an etch stop layer (not shown) positioned over an underlying via insulator level 34/94 (see col. 6, lines 25-46).

Goldberg is silent about the air gap extending below the lower surface of the at least one of the first and second interconnects by a distance corresponding to a thickness of the etch stop layer.

However, since the etch stop being formed above the underlying via insulator level 34/94, when the etching process is performed, it can be controlled to stop when it reaches the etch stop layer, or when it just goes through the etch stop layer. For example, as described in col. 6, lines 25-33, after forming the passivation layer 32, the etch stop layer, and the dielectric layer 36 over the interconnect 30, the etching process is controlled to perform an etch that exposes the interconnect 30. Thus, the etching process can be controlled to go through the etch stop layer. Furthermore, according to col. 9, lines 19-34, the air gap can be formed to extend to various deeps within the multiple interconnect level 20/34/36 or 89/94/104. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the etch process can be controlled to extend just through the etch stop layer in order to obtain an optimum isolation or reduction of capacitance coupling of the interconnects

within the dielectric layer 36 or 94; but not too far to the dielectric layer 34 or 20 to cause possible damage or crack to layer 34 or 20. In the other words, it would have been obvious to one of ordinary skills in the art to form the air gap extending below the lower surface of the at least one of the first and second interconnects by a distance corresponding to a thickness of the etch stop layer. See further col. 9, lines 49-54; col. 15, lines 8-28.

Regarding claim 5, Goldberg discloses the semiconductor device wherein the etch stop layer comprises silicon carbide. See col. 6, lines 25-33.

Regarding claim 6, Goldberg discloses the semiconductor device wherein the underlying via insulator level comprises silicon dioxide or fluorinated silicon dioxide. See col. 3, lines 31-45.

Conclusion

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-

1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

Dao H. Nguyen
Art Unit 2818
April 28, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800